Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listings of Claims:

1. (canceled)

2. (new) A family of transistor devices formed in a semiconductor substrate, the substrate being doped with P-type impurity and not comprising an epitaxial layer, the family of transistor devices comprising at least a PNP bipolar transistor and a CMOS pair, the substrate comprising an isolation structure for electrically isolating transistor devices enclosed within the isolation structure from a portion of the substrate outside the isolation structure,

the isolation structure comprising:

a first N-type isolation region extending downward from a surface of the substrate, the first N-type isolation region comprising a first annular N well and a deep N layer, the first N-type isolation structure enclosing an isolated P region of the substrate; and

a second N well having a relatively deep central portion and relatively shallow side portions, the relatively shallow side portions underlying a field oxide layer, the relatively deep central portion underlying a first opening in the field oxide layer, the second N well being electrically shorted to the first N-type isolation region;

the PNP bipolar transistor being located in the isolated P region of the substrate and comprising:

a first P well adjacent the surface of the substrate, the first P well forming a collector of the PNP bipolar transistor;

an N-type base region located adjacent the surface of the substrate within the first P well, the N-type base region forming a base of the PNP bipolar transistor; and

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a P-type region located adjacent the surface of the substrate within the N-type base region, the P-type region forming an emitter of the PNP bipolar transistor;

the CMOS pair comprising a PMOS and an NMOS, the PMOS being located in the second N well and comprising:

a first gate separated from the substrate by a first gate oxide layer;

a P-type source region located at the surface of the substrate in the second N well on one side of the first gate; and

a P-type drain region located at the surface of the substrate in the second N well on an opposite the of the first gate from the P-type source region; and

the NMOS being formed in a second P well, the second P well having a relatively deep central portion and relatively shallow side portions, the relatively shallow side portions underlying the field oxide layer, the relatively deep central portion underlying a second opening in the field oxide layer, the NMOS comprising:

a second gate separated from the substrate by a second gate oxide layer;

an N-type source region located at the surface of the substrate in the second P well on one side of the second gate; and

an N-type drain region located at the surface of the substrate in the second P well on an opposite the of the second gate from the N-type source region.

3. (new) The family of transistor devices of Claim 2 wherein the deep N layer comprises a high energy phosphorus implant.

4. (new) The family of transistor devices of Claim 2 wherein a doping profile in a vertical cross section of the deep N layer is non-monotonic.

5. (new) The family of transistor devices of Claim 2 wherein the first annular N well comprises multiple phosphorus implants at differing energies.

6. (new) The family of transistor devices of Claim 2 wherein a doping profile in a vertical cross section of the first annular N well is non-monotonic and non-Gaussian.

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7. (new) The family of transistor devices of Claim 2 wherein the first annular N well vertically overlaps the deep N layer.

8. (new) The family of transistor devices of Claim 2 wherein a doping profile in a vertical cross section of the second N well not under the field oxide layer is similar to a doping profile in a vertical cross section of the first annular N well not under the field oxide layer.

9. (new) The family of transistor devices of Claim 8 wherein a doping profile in a vertical cross section of the second N well under the field oxide layer is similar to a doping profile in a vertical cross section of the first annular N well under the field oxide layer.

10. (new) The family of transistor devices of Claim 8 wherein a portion of the first annular N well not under the field oxide layer and a portion of the second N well not under the field oxide layer include a shallow threshold adjust implant.

11. (new) The family of transistor devices of Claim 2 wherein each of the first annular N well and the second N well comprises a relatively high doping concentration region located below a relatively low doping concentration region.

12. (new) The family of transistor devices of Claim 11 wherein each of the first annular N well and the second N well comprises multiple phosphorus implants at differing energies.

13. (new) The family of transistor devices of Claim 11 wherein the relatively high doping concentration region of each of the first annular and second N wells is closer to the surface of the substrate in regions under the field oxide layer than in regions not under the field oxide layer.

14. (new) The family of transistor devices of Claim 2 wherein each of the first and second P wells comprises a relatively high doping concentration region located below a relatively low doping concentration region.

15. (new) The family of transistor devices of Claim 14 wherein each of the first and second P wells comprises multiple boron implants at differing energies.

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16. (new) The family of transistor devices of Claim 14 wherein the relatively high doping concentration region of each of the first and second P wells is closer to the surface of the substrate in regions under the field oxide layer than in regions not under the field oxide layer.

17. (new) The family of transistor devices of Claim 2 wherein a peak doping concentration of the deep N layer is at a sufficient depth in the substrate that a portion of the first P well located over the deep N layer is not substantially counter-doped and converted to N-type material.

18. (new) The family of transistor devices of Claim 17 wherein a junction breakdown voltage of the first P well exceeds a specified minimum voltage of the collector with respect to the first N-type isolation region.

19. (new) The family of transistor devices of Claim 18 wherein the junction breakdown voltage of the first P well exceeds 7 volts.

20. (new) The family of transistor devices of Claim 2 wherein the deep N layer extends laterally so as to overlap the second N well thereby forming a second N-type isolation region enclosing and containing the PMOS, the second isolation region being electrically shorted to the isolation structure.

21. (new) The family of transistor devices of Claim 2 wherein the isolation structure further comprises a second N-type isolation region enclosing and containing the NMOS wherein the second P well has a junction breakdown voltage relative to the second N-type isolation region.

22. (new) The family of transistor devices of Claim 21 wherein the junction breakdown voltage of the second P well relative to the second N-type isolation region exceeds 7 volts.

23. (new) The family of transistor devices of Claim 21 wherein the junction breakdown voltage of the second P well relative to the second N-type isolation region exceeds 15 volts.

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24. (new) The family of transistor devices of Claim 2 further comprising a third annular N well, the deep N layer extending laterally to overlap the third annular N well so

as to form a second isolation region enclosing and containing the NMOS and to electrically short the second isolation region to the isolation structure, wherein the second P well has a junction breakdown voltage relative to the second isolation region.

25. (new) The family of transistor devices of Claim 24 wherein the junction breakdown voltage of the P well to the second isolation region exceeds 7 volts.

26. (new) The family of transistor devices of Claim 24 wherein the junction breakdown voltage of the P well to the second isolation region exceeds 15 volts.

27. (new) The family of transistor devices of Claim 2 wherein the isolation structure has a breakdown voltage relative to a portion of the substrate outside the isolation structure exceeding some specified voltage.

28. (new) The family of transistor devices of Claim 27 wherein the breakdown voltage relative to a portion of the substrate outside the isolation structure exceeds 7 volts.

29. (new) The family of transistor devices of Claim 27 wherein the breakdown voltage relative to a portion of the substrate outside the isolation structure exceeds 15 volts.

30. (new) The family of transistor devices of Claim 27 wherein the breakdown voltage relative to a portion of the substrate outside the isolation structure exceeds 30 volts.

31. (new) The family of transistor devices of Claim 2 wherein each of the first and second P wells comprises a relatively high doping concentration region located below a relatively low doping concentration region and wherein the depth of the relatively high concentration region of the first and second P wells is sufficient to avoid substantial counterdoping of the base region of the PNP bipolar transistor.

32. (new) The family of transistor devices of Claim 2 comprising sidewall oxide spacers on the sides of the first and second gates.

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33. (new) The family of transistor devices of Claim 32 wherein the drain-to-source breakdown voltage of each of the NMOS and the PMOS in the off condition exceeds 7 volts.

34. (new) The family of transistor devices of Claim 2 comprising a P-type lightly-doped drain extension at the surface of the substrate between the first gate and the P-type drain region in the PMOS and an N-type lightly-doped drain extension at the surface of the substrate between the second gate and the N-type drain region in the NMOS.

35. (new) The family of transistor devices of Claim 34 wherein the drain-to-source breakdown voltage of each of the NMOS and the PMOS in the off condition exceeds 15 volts.

36. (new) The family of transistor devices of Claim 2 comprising a P-type lightly-doped drain extension at the surface of the substrate between the first gate and the P-type drain region in the PMOS and an N-type lightly-doped drain extension at the surface of the substrate between the second gate and the N-type drain region in the NMOS and a P-type lightly-doped source extension at the surface of the substrate between the first gate and the P-type source region in the PMOS and an N-type lightly-doped source extension at the surface of the substrate between the second gate and the N-type source region in the NMOS.

37. (new) The family of transistor devices of Claim 36 wherein the drain-to-body and source-to-body breakdown voltages of each of the NMOS and the PMOS in the off condition exceeds 15 volts.

38. (new) The family of transistor devices of Claim 2 wherein the NMOS includes a phosphorus ESD implant.

39. (new) The family of transistor devices of Claim 38 wherein a doping profile in a vertical cross section of the ESD implant is similar to a doping profile in a vertical cross section of the N-type base region of the PNP bipolar transistor.

40. (new) A family of transistor devices formed in a semiconductor substrate, the substrate being doped with P-type impurity and not comprising an epitaxial layer, the family of transistor devices comprising at least complementary NPN and PNP bipolar transistors and a CMOS pair, the substrate comprising an isolation structure for electrically isolating transistor devices enclosed within the isolation structure from a portion of the substrate outside the isolation structure,

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the isolation structure comprising:

a first N-type isolation region extending downward from a surface of the substrate, the first N-type isolation region comprising a first annular N well and a deep N layer, the first N-type isolation structure enclosing an isolated P region of the substrate; and

a second N well located at the surface of the substrate outside the first N-type isolation region and the isolated P region;

the PNP bipolar transistor being located in the isolated P region of the substrate and comprising:

a first P well adjacent the surface of the substrate, the first P well forming a collector of the PNP bipolar transistor;

an N-type base region located adjacent the surface of the substrate within the first P well, the N-type base region forming a base of the PNP bipolar transistor; and

a P-type region located adjacent the surface of the substrate within the N-type base region, the P-type region forming an emitter of the PNP bipolar transistor;

the CMOS pair comprising a PMOS and an NMOS, the PMOS comprising:

a third N well having a relatively deep central portion and relatively shallow side portions, the relatively shallow side portions underlying a field oxide layer, the relatively deep central portion underlying a first opening in the field oxide layer;

a first gate separated from the substrate by a first gate oxide layer;

a P-type source region located at the surface of the substrate in the third N well on one side of the first gate; and

a P-type drain region located at the surface of the substrate in the third N well on an opposite side the of the first gate from the P-type source region;

the NMOS comprising:

a second P well having a relatively deep central portion and relatively shallow side portions, the relatively shallow side portions underlying the field

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oxide layer, the relatively deep central portion underlying a second opening in the field oxide layer;

a second gate separated from the substrate by a second gate oxide layer;

an N-type source region located at the surface of the substrate in the second P well on one side of the second gate; and

an N-type drain region located at the surface of the substrate in the second P well on an opposite the of the second gate from the N-type source region; and

the NPN bipolar transistor comprising:

the second N well, the second N well electrically isolating the NPN bipolar transistor from a portion of the substrate outside the second N well , the second N well forming the collector of the NPN bipolar transistor;

a third P well located at the surface of the substrate within the second N well, the third P well forming the base of the NPN bipolar transistor; and

a second N-type region located at the surface of the substrate within the third P well, the second N-type region forming the emitter of the NPN bipolar transistor.

41. (new) The family of transistor devices of Claim 40 wherein the deep N layer comprises a high energy phosphorus implant.

42. (new) The family of transistor devices of Claim 40 wherein a doping profile in a vertical cross section of the deep N layer is non-monotonic.

43. (new) The family of transistor devices of Claim 40 wherein the first annular N well comprises multiple phosphorus implants at differing energies.

44. (new) The family of transistor devices of Claim 40 wherein a doping profile in a vertical cross section of the first annular N well is non-monotonic and non-Gaussian.

45. (new) The family of transistor devices of Claim 40 wherein the first annular N well vertically overlaps the deep N layer.

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46. (new) The family of transistor devices of Claim 40 wherein a doping profile in a vertical cross section of the second N well not under the field oxide layer is similar to a doping profile in a vertical cross section of the first annular N well not under the field oxide layer.

47. (new) The family of transistor devices of Claim 46 wherein a doping profile in a vertical cross section of the second N well under the field oxide layer is similar to a doping profile in a vertical cross section of the first annular N well under the field oxide layer.

48. (new) The family of transistor devices of Claim 40 wherein a doping profile in a vertical cross section of the second P well under the field oxide layer is similar to a doping profile in a vertical cross section of the first P well under the field oxide layer.

49. (new) The family of transistor devices of Claim 40 wherein a doping profile in a vertical cross section of the first P well not under the field oxide layer is similar to a doping profile in a vertical cross section of the third P well not under the field oxide layer.

50. (new) The family of transistor devices of Claim 40 wherein a doping profile in a vertical cross section of the second P well not under the field oxide layer is similar to a doping profile in a vertical cross section of the third P well not under the field oxide layer.

51. (new) The family of transistor devices of Claim 40 wherein a doping profile in a vertical cross section of the first P well not under the field oxide layer is similar to a doping profile in a vertical cross section of the second P well not under the field oxide layer and the doping profile in a vertical cross section of the second P well not under the field oxide layer is similar to a doping profile in a vertical cross section of the third P well not under the field oxide layer.

52. (new) The family of transistor devices of Claim 40 wherein each of the first annular N well and the second N well comprises a relatively high doping concentration region located below a relatively low doping concentration region.

53. (new) The family of transistor devices of Claim 52 wherein each of the first annular N well and the second N well comprises multiple phosphorus implants at differing energies.

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54. (new) The family of transistor devices of Claim 52 wherein the relatively high doping concentration region of each of the first annular and second N wells is closer to the surface of the substrate in regions under the field oxide layer than in regions not under the field oxide layer.

55. (new) The family of transistor devices of Claim 40 wherein each of the first, second and third P wells comprises a relatively high doping concentration region located below a relatively low doping concentration region.

56. (new) The family of transistor devices of Claim 55 wherein each of the first, second and third P wells comprises multiple boron implants at differing energies.

57. (new) The family of transistor devices of Claim 55 wherein the relatively high doping concentration region of each of the first, second and third P wells is closer to the surface of the substrate in regions under the field oxide layer than in regions not under the field oxide layer.

58. (new) The family of transistor devices of Claim 40 wherein a peak doping concentration of the deep N layer is at a sufficient depth in the substrate that a portion of the first P well located over the deep N layer is not substantially counter-doped and converted to N-type material.

59. (new) The family of transistor devices of Claim 58 wherein a junction breakdown voltage of the first P well exceeds a specified minimum voltage of the collector with respect to the first N-type isolation region.

60. (new) The family of transistor devices of Claim 59 wherein the junction breakdown voltage of the first P well exceeds 7 volts.

61. (new) The family of transistor devices of Claim 40 wherein the deep N layer extends laterally to a location below the NPN bipolar transistor and wherein a peak doping concentration of the deep N layer is at a sufficient depth in the substrate that a portion of the third P well located over the deep N layer is not substantially counter-doped and converted to N-type material.

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62. (new) The family of transistor devices of Claim 61 wherein a junction breakdown voltage of the third P well exceeds a specified minimum voltage of the base of the PNP bipolar transistor with respect to the first N-type isolation region.

63. (new) The family of transistor devices of Claim 62 wherein the junction breakdown voltage of the third P well exceeds 7 volts.

64. (new) The family of transistor devices of Claim 40 further comprising a fourth annular N well, the deep N layer extending laterally to overlap the fourth annular N well so as to form a second N-type isolation region enclosing and containing the PMOS and to electrically short the second N-type isolation region to the isolation structure.

65. (new) The family of transistor devices of Claim 40 further comprising a fourth annular N well, the deep N layer extending laterally to overlap the fourth annular N well so as to form a second N-type isolation region enclosing and containing the NMOS and to electrically short the second N-type isolation region to the isolation structure, the second P well having a junction breakdown voltage relative to the second N-type isolation structure.

66. (new) The family of transistor devices of Claim 65 wherein the junction breakdown voltage of the second P well relative to the second N-type isolation structure exceeds 7 volts.

67. (new) The family of transistor devices of Claim 65 wherein the junction breakdown voltage of the second P well relative to the second N-type isolation structure exceeds 15 volts.

68. (new) The family of transistor devices of Claim 40 further comprising a fourth annular N well, the deep N layer extending laterally to overlap the fourth annular N well so as to form a second N-type isolation region enclosing and containing the NMOS and the PMOS and to electrically short the second N-type isolation region to the isolation structure, the second P well having a junction breakdown voltage relative to the second N-type isolation structure.

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69. (new) The family of transistor devices of Claim 68 wherein the junction breakdown voltage of the second P well relative to the second N-type isolation structure exceeds 7 volts.

70. (new) The family of transistor devices of Claim68 wherein the junction breakdown voltage of the second P well relative to the second N-type isolation structure exceeds 15 volts.

71. (new) The family of transistor devices of Claim 40 wherein the isolation structure has a breakdown voltage relative to the portion of the substrate outside the isolation structure exceeding a specified voltage.

72. (new) The family of transistor devices of Claim 71 wherein the breakdown voltage of the isolation structure relative to the portion of the substrate outside the isolation structure exceeds 7 volts.

73. (new) The family of transistor devices of Claim 71 wherein the breakdown voltage of the isolation structure relative to the portion of the substrate outside the isolation structure exceeds 15 volts.

74. (new) The family of transistor devices of Claim 71 wherein the breakdown voltage of the isolation structure relative to the portion of the substrate outside the isolation structure exceeds 30 volts.

75. (new) The family of transistor devices of Claim 40 wherein each of the first, second and third P wells comprises a relatively high doping concentration region located below a relatively low doping concentration region and wherein a peak doping concentration of the high doping concentration region in the first P well is at a sufficient depth that the N-type base region within the first P well is not substantially counter-doped and converted to P-type material.

76. (new) The family of transistor devices of Claim 40 comprising sidewall oxide spacers on the sides of the first and second gates.

77. (new) The family of transistor devices of Claim 76 wherein the drain-to-source breakdown voltage of each of the NMOS and the PMOS in the off condition exceeds 7 volts.

78. (new) The family of transistor devices of Claim 40 comprising a P-type lightly-doped drain extension at the surface of the substrate between the first gate and the P-type

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drain region in the PMOS and an N-type lightly-doped drain extension at the surface of the substrate between the second gate and the N-type drain region in the NMOS.

79. (new) The family of transistor devices of Claim 78 wherein the drain-to-source breakdown voltage of each of the NMOS and the PMOS in the off condition exceeds 15 volts.

80. (new) The family of transistor devices of Claim 40 comprising a P-type lightly-doped drain extension at the surface of the substrate between the first gate and the P-type drain region in the PMOS and an N-type lightly-doped drain extension at the surface of the substrate between the second gate and the N-type drain region in the NMOS and a P-type lightly-doped source extension at the surface of the substrate between the first gate and the P-type source region in the PMOS and an N-type lightly-doped source extension at the surface of the substrate between the second gate and the N-type source region in the NMOS.

81. (new) The family of transistor devices of Claim 40 wherein the drain-to-body and source-to-body breakdown voltages of each of the NMOS and the PMOS in the off condition exceeds 15 volts.

82. (new) The family of transistor devices of Claim 40 wherein the NMOS includes a phosphorus ESD implant.

83. (new) The family of transistor devices of Claim 82 wherein a doping profile in a vertical cross section of the ESD implant is similar to a doping profile in a vertical cross section of the N-type base region of the PNP bipolar transistor.

84. (new) A family of transistor devices formed in a semiconductor substrate, the substrate being doped with P-type impurity and not comprising an epitaxial layer, the family of transistor devices comprising at least an NPN bipolar transistor and a CMOS pair, the substrate comprising an isolation structure for electrically isolating transistor devices enclosed within the isolation structure from a portion of the substrate outside the isolation structure,

the isolation structure comprising a first N-type isolation region extending downward from a surface of the substrate, the first N-type isolation region

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comprising a first annular N well and a deep N layer, the first N-type isolation structure enclosing an isolated P region of the substrate; and

the CMOS pair comprising a PMOS and an NMOS, the PMOS comprising:

a second N well having a relatively deep central portion and relatively shallow side portions, the relatively shallow side portions underlying a field oxide layer, the relatively deep central portion underlying a first opening in the field oxide layer;

a first gate separated from the substrate by a first gate oxide layer;

a P-type source region located at the surface of the substrate in the second N well on one side of the first gate; and

a P-type drain region located at the surface of the substrate in the second N well on an opposite the of the first gate from the P-type source region; and

the NMOS comprising:

a first P well, the first P well having a relatively deep central portion and relatively shallow side portions, the relatively shallow side portions underlying the field oxide layer, the relatively deep central portion underlying a second opening in the field oxide layer;

a second gate separated from the substrate by a second gate oxide layer;

an N-type source region located at the surface of the substrate in the first P well on one side of the second gate; and

an N-type drain region located at the surface of the substrate in the first P well on an opposite the of the second gate from the N-type source region; and

the NPN bipolar transistor comprising:

the first N-type isolation region, the first N-type isolation region forming a collector of the NPN bipolar transistor;

a P-type base region located adjacent the surface of the substrate within the isolated P region, the P-type base region forming at least a portion of a base of the NPN bipolar transistor; and

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an N-type region located adjacent the surface of the substrate within the P-type base region, the N-type region forming an emitter of the NPN bipolar transistor.

85. (new) The family of transistor devices of Claim 84 wherein the deep N layer comprises a high energy phosphorus implant.

86. (new) The family of transistor devices of Claim 84 wherein a doping profile in a vertical cross section of the deep N layer is non-monotonic.

87. (new) The family of transistor devices of Claim 84 wherein the first annular N well comprises multiple phosphorus implants at differing energies.

88. (new) The family of transistor devices of Claim 84 wherein a doping profile in a vertical cross section of the first annular N well is non-monotonic and non-Gaussian.

89. (new) The family of transistor devices of Claim 84 wherein the first annular N well vertically overlaps the deep N layer.

90. (new) The family of transistor devices of Claim 84 wherein a doping profile in a vertical cross section of the second N well not under the field oxide layer is similar to a doping profile in a vertical cross section of the first annular N well not under the field oxide layer.

91. (new) The family of transistor devices of Claim 84 wherein a doping profile in a vertical cross section of the second N well under the field oxide layer is similar to a doping profile in a vertical cross section of the first annular N well under the field oxide layer.

92. (new) The family of transistor devices of Claim 84 wherein a doping profile in a vertical cross section of the first P well not under the field oxide layer is similar to a doping profile in a vertical cross section of the third P well not under the field oxide layer.

93. (new) The family of transistor devices of Claim 84 wherein each of the first annular N well and the second N well comprises a relatively high doping concentration region located below a relatively low doping concentration region.

94. (new) The family of transistor devices of Claim 93 wherein each of the first annular N well and the second N well comprises multiple phosphorus implants at differing energies.

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95. (new) The family of transistor devices of Claim 93 wherein the relatively high doping concentration region of each of the first annular and second N wells is closer to the surface of the substrate in regions under the field oxide layer than in regions not under the field oxide layer.

96. (new) The family of transistor devices of Claim 84 wherein each of the first and second P wells comprises a relatively high doping concentration region located below a relatively low doping concentration region.

97. (new) The family of transistor devices of Claim 96 wherein each of the first and second P wells comprises multiple boron implants at differing energies.

98. (new) The family of transistor devices of Claim 96 wherein the relatively high doping concentration region of each of the first and second P wells is closer to the surface of the substrate in regions under the field oxide layer than in regions not under the field oxide layer.

99. (new) The family of transistor devices of Claim 84 wherein a peak doping concentration of the deep N layer is at a sufficient depth in the substrate that a portion of the P-type base region located over the deep N layer is not substantially counter-doped and converted to N-type material.

100. (new) The family of transistor devices of Claim 84 wherein the deep N layer extends laterally so as to overlap the second N well thereby forming a second N-type isolation region enclosing and containing the PMOS, the second N-type isolation region being electrically shorted to the isolation structure.

101. (new) The family of transistor devices of Claim 84 wherein the isolation structure further comprises a second N-type isolation region enclosing and containing the NMOS wherein the first P well has a junction breakdown voltage relative to the second N-type isolation region.

102. (new) The family of transistor devices of Claim 101 wherein the junction breakdown voltage of the first P well relative to second N-type isolation region exceeds 7 volts.

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103. (new) The family of transistor devices of Claim 101 wherein the junction breakdown voltage of the first P well relative to second N-type isolation region exceeds 15 volts.

104. (new) The family of transistor devices of Claim 84 further comprising a third annular N well, the deep N layer extending laterally to overlap the third annular N well so as to form a second N-type isolation region enclosing and containing the NMOS and the PMOS and to electrically short the second N-type isolation region to the isolation structure, the first P well having a junction breakdown voltage relative to the second N-type isolation region.

105. (new) The family of transistor devices of Claim 104 wherein the junction breakdown voltage of the first P well relative to the second N-type isolation region exceeds 7 volts.

106. (new) The family of transistor devices of Claim104 wherein the junction breakdown voltage of the first P well relative to the second N-type isolation region exceeds 15 volts.

107. (new) The family of transistor devices of Claim 84 wherein the isolation structure has a breakdown voltage relative to a portion of the substrate outside the isolation structure exceeding some specified voltage.

108. (new) The family of transistor devices of Claim 107 wherein the breakdown voltage relative to a portion of the substrate outside the isolation structure exceeds 7 volts.

109. (new) The family of transistor devices of Claim 107 wherein the breakdown voltage relative to a portion of the substrate outside the isolation structure exceeds 15 volts.

110. (new) The family of transistor devices of Claim107 wherein the breakdown voltage relative to a portion of the substrate outside the isolation structure exceeds 30 volts.

111. (new) The family of transistor devices of Claim 84 comprising sidewall oxide spacers on the sides of the first and second gates.

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112. (new) The family of transistor devices of Claim 111 wherein the drain-to-source breakdown voltage of each of the NMOS and the PMOS in the off condition exceeds 7 volts.

113. (new) The family of transistor devices of Claim 84 comprising a P-type lightly-doped drain extension at the surface of the substrate between the first gate and the P-type drain region in the PMOS and an N-type lightly-doped drain extension at the surface of the substrate between the second gate and the N-type drain region in the NMOS.

114. (new) The family of transistor devices of Claim 113 wherein the drain-to-source breakdown voltage of each of the NMOS and the PMOS in the off condition exceeds 15 volts.

115. (new) The family of transistor devices of Claim 84 comprising a P-type lightly-doped drain extension at the surface of the substrate between the first gate and the P-type drain region in the PMOS and an N-type lightly-doped drain extension at the surface of the substrate between the second gate and the N-type drain region in the NMOS and a P-type lightly-doped source extension at the surface of the substrate between the first gate and the P-type source region in the PMOS and an N-type lightly-doped source extension at the surface of the substrate between the second gate and the N-type source region in the NMOS.

116. (new) The family of transistor devices of Claim 115 wherein the drain-to-body and source-to-body breakdown voltages of each of the NMOS and the PMOS in the off condition exceeds 15 volts.

117. (new) The family of transistor devices of Claim 84 wherein the NMOS includes a phosphorus ESD implant.

118. (new) The family of transistor devices of Claim 117 wherein a doping profile in a vertical cross section of the ESD implant is similar to a doping profile in a vertical cross section of the N-type base region of the PNP bipolar transistor.

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119. (new) A family of transistor devices formed in a semiconductor substrate, the substrate being doped with P-type impurity and not comprising an epitaxial layer, the family of transistor devices comprising at least one NPN bipolar transistor and at least two

CMOS pairs, the substrate comprising an isolation structure for electrically isolating transistor devices enclosed within the isolation structure from a portion of the substrate outside the isolation structure,

the isolation structure comprising a first N-type isolation region extending downward from a surface of the substrate, the first N-type isolation region comprising a first annular N well and a deep N layer, the first N-type isolation structure enclosing an isolated P region of the substrate;

the family of transistor devices further comprising:

a first CMOS pair comprising a first PMOS and a first NMOS, the first PMOS comprising:

a second N well having a relatively deep central portion and relatively shallow side portions, the relatively shallow side portions underlying a field oxide layer, the relatively deep central portion underlying a first opening in the field oxide layer, the second N well having a first vertical distribution of dopant;

a first gate separated from the substrate by a first gate dielectric layer;

a first P-type source region located at the surface of the substrate in the second N well on one side of the first gate; and

a first P-type drain region located at the surface of the substrate in the second N well on an opposite the of the first gate from the first P-type source region; and

the first NMOS comprising:

a first P well, the first P well having a relatively deep central portion and relatively shallow side portions, the relatively shallow side portions underlying the field oxide layer, the relatively deep central portion underlying a second opening in the field oxide layer, the first P well having a second vertical distribution of dopant;

a second gate separated from the substrate by a second gate dielectric layer;

a first N-type source region located at the surface of the substrate in the first P well on one side of the second gate; and

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a first N-type drain region located at the surface of the substrate in the first P well on an opposite the of the second gate from the first N-type source region;

a second CMOS pair comprising a second PMOS and a second NMOS, the second PMOS comprising:

a third N well having a relatively deep central portion and relatively shallow side portions, the relatively shallow side portions underlying a field oxide layer, the relatively deep central portion underlying a third opening in the field oxide layer, the third N well having a third vertical distribution of dopant different from the first vertical distribution of dopant;

a third gate separated from the substrate by a third gate dielectric layer;

a second P-type source region located at the surface of the substrate in the third N well on one side of the third gate; and

a second P-type drain region located at the surface of the substrate in the third N well on an opposite the of the third gate from the second P-type source region; and

the second NMOS comprising:

a second P well, the second P well having a relatively deep central portion and relatively shallow side portions, the relatively shallow side portions underlying the field oxide layer, the relatively deep central portion underlying a fourth opening in the field oxide layer, the second P well having a fourth vertical distribution of dopant different from the second vertical distribution of dopant;

a fourth gate separated from the substrate by a fourth gate dielectric layer;

a second N-type source region located at the surface of the substrate in the second P well on one side of the fourth gate; and

a second N-type drain region located at the surface of the substrate in the second P well on an opposite the of the fourth gate from the second N-type source region; and

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an NPN bipolar transistor comprising:

the first N-type isolation region, the first N-type isolation region forming a collector of the NPN bipolar transistor;

a P-type base region located adjacent the surface of the substrate within the isolated P region, the P-type base region forming at least a portion of a base of the NPN bipolar transistor; and

an N-type region located adjacent the surface of the substrate within the P-type base region, the N-type region forming an emitter of the NPN bipolar transistor.

120. (new) The family of transistor devices of Claim 119 wherein the deep N layer comprises a high energy phosphorus implant.

121. (new) The family of transistor devices of Claim 119 wherein a doping profile in a vertical cross section of the deep N layer is non-monotonic.

122. (new) The family of transistor devices of Claim 119 wherein the first annular N well comprises multiple phosphorus implants at differing energies.

123. (new) The family of transistor devices of Claim 119 wherein a doping profile in a vertical cross section of the first annular N well is non-monotonic and non-Gaussian.

124. (new) The family of transistor devices of Claim 119 wherein the first annular N well vertically overlaps the deep N layer.

125. (new) The family of transistor devices of Claim 119 wherein a doping profile in a vertical cross section of the second N well not under the field oxide layer is similar to a doping profile in a vertical cross section of the first annular N well not under the field oxide layer.

126. (new) The family of transistor devices of Claim 119 wherein a vertical dopant distribution of a portion of the first annular N well not under the field oxide layer is substantially equal to the sum of a vertical dopant distribution of the relatively deep central portion of the second N well and a vertical dopant distribution of the relatively deep central portion of the third N well.

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127. (new) The family of transistor devices of Claim 119 wherein the relatively deep central portion of the third N well is deeper than the relatively deep central portion of the second N well.

128. (new) The family of transistor devices of Claim 119 wherein a surface doping concentration of the relatively deep central portion of the third N well is lower than a surface doping concentration of the relatively deep central portion of the second N well.

129. (new) The family of transistor devices of Claim 119 wherein the first gate oxide layer is thinner than the third gate oxide layer.

130. (new) The family of transistor devices of Claim 119 wherein the first PMOS comprises a first threshold adjust implant and the second PMOS comprises a second threshold adjust implant, a vertical dopant distribution of the first threshold adjust implant being different from a vertical dopant distribution of the second threshold adjust implant.

131. (new) The family of transistor devices of Claim119 comprising sidewall oxide spacers on the sides of the first gate.

132. (new) The family of transistor devices of Claim 119 wherein the first PMOS has a junction breakdown voltage exceeding 7 volts.

133. (new) The family of transistor devices of Claim119 wherein the first PMOS has a drain to source breakdown rating in the off condition of at least 7 volts.

134. (new) The family of transistor devices of Claim 119 wherein the second PMOS comprises a P-type lightly-doped drain extension at the surface of the substrate between the third gate and the second P-type drain region.

135. (new) The family of transistor devices of Claim 134 wherein a doping concentration of the P-type lightly-doped drain extension is less than a doping concentration of the second P-type drain region.

136. (new) The family of transistor devices of Claim 119 wherein the second PMOS has a drain to body junction breakdown voltage exceeding 15 volts.

137. (new) The family of transistor devices of Claim 119 the second PMOS has a drain to source breakdown rating in the off condition of at least 15 volts,

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138. (new) The family of transistor devices of Claim 119 wherein each of the first annular, second and third N wells comprises a relatively high doping concentration region located below a relatively low doping concentration region.

139. (new) The family of transistor devices of Claim 138 wherein the field oxide layer laterally surrounding the third opening overlies a portion of each of the second and third N wells.

140. (new) The family of transistor devices of Claim 139 wherein the relatively shallow side portions of the second N well do not extend to areas not under the field-oxide layer.

141. (new) The family of transistor devices of Claim 138 wherein the relatively high doping concentration region of each of the first annular and second N wells is closer to the surface of the substrate in regions under the field oxide layer than in regions not under the field oxide layer.

142. (new) The family of transistor devices of Claim 119 wherein the relatively deep central portion of the second P well is deeper than the relatively deep central portion of the first P well.

143. (new) The family of transistor devices of Claim 119 wherein a surface doping concentration of the relatively deep central portion of the second P well is lower than a surface doping concentration of the relatively deep central portion of the first P well.

144. (new) The family of transistor devices of Claim 119 wherein the fourth gate oxide layer is thicker than the second gate oxide layer.

145. (new) The family of transistor devices of Claim 119 wherein the first NMOS comprises a first threshold adjust implant and the second NMOS comprises a second threshold adjust implant, a vertical dopant distribution of the first threshold adjust implant being different from a vertical dopant distribution of the second threshold adjust implant.

146. (new) The family of transistor devices of Claim 119 comprising sidewall oxide spacers on the sides of the second gate.

147. (new) The family of transistor devices of Claim 119 wherein the first NMOS has a drain to body junction breakdown voltage exceeding 7 volts.

148. (new) The family of transistor devices of Claim 119 wherein the first NMOS has a drain to source breakdown rating in the off condition of at least 7 volts.

149. (new) The family of transistor devices of Claim 119 comprising a N-type lightly-doped drain extension at the surface of the substrate between the fourth gate and the second N-type drain region in the second NMOS.

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150. (new) The family of transistor devices of Claim 149 wherein the N-type lightly-doped drain extension has a lower doping concentration than the second N-type drain region.

151. (new) The family of transistor devices of Claim 119 wherein the second NMOS has a junction breakdown voltage exceeding 15 volts.

152. (new) The family of transistor devices of Claim 119 where the second NMOS has a drain to source breakdown rating in the off condition of at least 15 volts.

153. (new) The family of transistor devices of Claim 119 wherein each of the first and second P wells comprises a relatively high doping concentration region located below a relatively low doping concentration region.

154. (new) The family of transistor devices of Claim 153 wherein the field oxide layer laterally surrounding the fourth opening overlies a portion of each of the first and the second P wells.

155. (new) The family of transistor devices of Claim 154 wherein the relatively shallow side portions of the first P well do not extend to areas not under the field-oxide layer.

156. (new) The family of transistor devices of Claim 153 wherein the relatively high doping concentration region of each of the first and second P wells is closer to the surface of the substrate in regions under the field oxide layer than in regions not under the the field oxide layer.

157. (new) The family of transistor devices of Claim 119 wherein the first and third gates comprise the same material.

158. (new) The family of transistor devices of Claim 157 wherein the first NMOS and the first PMOS comprise similar threshold adjust implants.

159. (new) The family of transistor devices of Claim 119 wherein the second and fourth gates comprise the same material.

160. (new) The family of transistor devices of Claim 159 wherein the second NMOS and the second PMOS comprise similar threshold adjust implants.

161. (new) The family of transistor devices of Claim 119 wherein the first, second, third and fourth gates comprise the same material.

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162. (new) The family of transistor devices of Claim 119 wherein the first PMOS, second PMOS, first NMOS and second NMOS comprise similar threshold adjust implants.

163. (new) The family of transistor devices of Claim 162 wherein the similar threshold adjust implants are formed by a blanket implant into only those areas of the substrate not covered by the field oxide layer.

164. (new) The family of transistor devices of Claim 119 wherein the first gate dielectric layer and the third gate dielectric layer have the some thickness and comprise the same material.

165. (new) The family of transistor devices of Claim 119 wherein the second gate dielectric layer and the fourth gate dielectric layer have the some thickness and comprise the same material.

166. (new) The family of transistor devices of Claim 119 wherein a vertical dopant distribution of a portion of the P-type base region not under the field oxide layer is similar to a vertical dopant distribution of the relatively deep central portions of each of the first and second P wells.

167. (new) The family of transistor devices of Claim 119 further comprising a second N-type isolation region and a PNP bipolar transistor, the second N-type isolation region enclosing a second isolated P region of the substrate, the PNP bipolar transistor being formed in the second isolated P region and comprising:

a third P well adjacent the surface of the substrate, the third P well forming a collector of the PNP bipolar transistor;

an N-type base region located adjacent the surface within the third P well, the N-type base region forming a base of the PNP bipolar transistor; and

a P-type region located adjacent the surface of the substrate within the N-type base region, the P-type region forming an emitter of the PNP bipolar transistor.

168. (new) The family of transistor devices of Claim167 wherein a vertical dopant distribution of the third P well not under the field oxide layer is similar to a vertical dopant distribution of the relatively deep central portion of each of the first and the second P wells.

169. (new) The family of transistor devices of Claim167 wherein a vertical dopant distribution of a portion of the P-type base region not under the field oxide layer is similar

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to a vertical dopant distribution of a portion of the third P well not under the field oxide layer.

170. (new) The family of transistor devices of Claim 167 wherein a vertical dopant distribution of a portion of the P-type base region not under the field oxide layer is similar to a vertical dopant distribution of each of a portion of the third P well not under the field oxide layer, the relatively deep central portion of the first P well, and the relatively deep central portion of the second P well.

171. (new) The family of transistor devices of Claim 119 further comprising a second isolation structure including a fourth N well having a vertical dopant distribution similar to the vertical dopant distribution of the first annular N well, wherein the second isolation structure encloses the first PMOS, wherein the deep N layer extends laterally to overlap the fourth N well, thereby electrically shorting the second isolation structure to the isolation structure.

172. (new) The family of transistor devices of Claim 171 further comprising a third isolation structure including a fifth N well having a vertical dopant distribution similar to the vertical dopant distribution of the first annular N well, wherein the third isolation structure encloses the second PMOS, wherein the deep N layer extends laterally to overlap the fifth N well, thereby electrically shorting the third isolation structure to the isolation structure.

173. (new) The family of transistor devices of Claim 172 further comprising a fourth isolation structure including a sixth N well having a vertical dopant distribution similar to the vertical dopant distribution of the first annular N well, wherein the fourth isolation structure encloses the first NMOS, wherein the deep N layer extends laterally to overlap the sixth N well, thereby electrically shorting the fourth isolation structure to the isolation structure.

174. (new) The family of transistor devices of Claim 173 further comprising a fifth isolation structure including a seventh N well having a vertical dopant distribution similar to the vertical dopant distribution of the first annular N well, wherein the fifth isolation structure encloses the second NMOS, wherein the deep N layer extends laterally to overlap the seventh N well, thereby electrically shorting the fifth isolation structure to the isolation structure.

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175. (new) The family of transistor devices of Claim 119 further comprising a second isolation structure including a fourth N well having a vertical dopant distribution similar to the vertical dopant distribution of the first annular N well, wherein the second isolation structure encloses the first PMOS and first NMOS, wherein the deep N layer extends laterally to overlap the fourth N well, thereby electrically shorting the second isolation structure to the isolation structure.

176. (new) The family of transistor devices of Claim 119 further comprising a second isolation structure including a fourth N well having a vertical dopant distribution similar to the vertical dopant distribution of the first annular N well, wherein the second isolation structure encloses the second PMOS and second NMOS, wherein the deep N layer extends laterally to overlap the fourth N well, thereby electrically shorting the second isolation structure to the isolation structure.

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